AF/2811

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Ashraf W. Lotfi, *et al.*
Serial No.:	09/448,856
Filed:	November 23, 1999
Title:	SiC NMOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME
Group:	2811
Examiner:	Ori Nadav

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Mail Stop Appeal Brief-Patents

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March 31, 2004 / Elizabeth Shumaker
Date of Mailing / Signature of person mailing

ATTENTION: Board of Patent Appeals and Interferences

Sirs:

APPELLANT'S BRIEF UNDER 37 C.F.R. §1.192

This is an appeal from a Final Rejection dated November 3, 2003, of Claims 44-47 and 49-54. The Appellants submit this Brief in triplicate as required by 37 C.F.R. §1.192(a), with the statutory fee of $ 330.00 as set forth in 37 C.F.R.§1.17(c), and hereby authorize the Commissioner

to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 08-2395.

This Brief contains these items under the following headings, and in the order set forth below in accordance with 37 C.F.R. §1.192(c):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF INVENTION

VI. ISSUES

VII. GROUPING OF CLAIMS

VIII. PRIOR ART

IX. APPELLANTS' ARGUMENTS

X. APPENDIX A - CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this appeal is the Assignee, Agere Systems, Inc.

II. RELATED APPEALS AND INTERFERENCES

No other appeals or interferences will directly affect, be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF THE CLAIMS

Claims 44-47 and 49-54 are pending in this Application.

IV. STATUS OF THE AMENDMENTS

The present Application was filed on November 23, 1999. The Appellants filed a first Amendment on April 30, 2001, in response to an Examiner's Action mailed February 14, 2001. The Examiner entered the first Amendment and subsequently issued a Final Rejection on June 15, 2001. The Appellants then filed a second Amendment on August 9, 2001, in response to the Final Rejection. The Examiner did not enter the second Amendment and subsequently issued an Advisory Action on September 26, 2001. The Appellants then filed a Request for Continued Examination on October 8, 2001, with a preliminary amendment entering the amendments made in response to the

Final Rejection of June 15, 2001. The Examiner then issued a third (non-final) Rejection on December 13, 2001. The Appellants then filed a third Amendment on June 13, 2002. The Examiner entered the third Amendment and subsequently issued a second Final Rejection on October 11, 2002. The Appellants then filed a fourth Amendment on December 16, 2002, in response to the second Final Rejection. The Examiner did not enter the fourth Amendment and subsequently issued an Advisory Action on December 23, 2002. The Appellants then filed a Request for Continued Examination on January 10, 2003, with a preliminary amendment entering the amendments made in response to the second Final Rejection of October 11, 2002. The Examiner then issued a fifth (non-final) Rejection on May 30, 2003. The Appellants then filed a fifth Response on August 29, 2003. The Examiner subsequently issued a third Final Rejection on November 3, 2003. The Appellants then filed a sixth Response on December 10, 2003, in response to the third Final Rejection. The Examiner indicated that the response to the third Final Rejection did not place the Application in condition for allowance, and issued a third Advisory Action on January 23, 2004. The Appellants then filed a Notice of Appeal on February 3, 2004.

V. SUMMARY OF THE INVENTION

The present invention provides a semiconductor device, including a silicon carbide metal oxide semiconductor field effect transistor (MOSFET). (Summary) As shown in connection with Illustrations 1 & 2 below (FIG.s 3A & 2F, respectively), the semiconductor device 300 includes both a silicon carbide lateral MOSFET 307 and silicon CMOS devices 334, 345. As shown in Illustration 1, the silicon carbide lateral MOSFET 307 includes a silicon carbide tub 310 located over a

conductive substrate 305. The silicon carbide lateral MOSFET 307 further includes a gate 321 formed over the silicon carbide tub 310, and source and drain regions 325, 330 located in the silicon carbide tub 310 and laterally offset from the gate 321. As shown in Illustration 2, the silicon carbide tub 310 may be located within a trench 209 in the conductive substrate 205. Located proximate the silicon carbide lateral MOSFET 307 on the conductive substrate 305 are the silicon CMOS devices 334, 345. In accordance with the principles of the present invention, the silicon CMOS devices 334, 345 have tubs 335, 340, comprising a material different from the silicon carbide tub 310, 210.

FIG. 3A

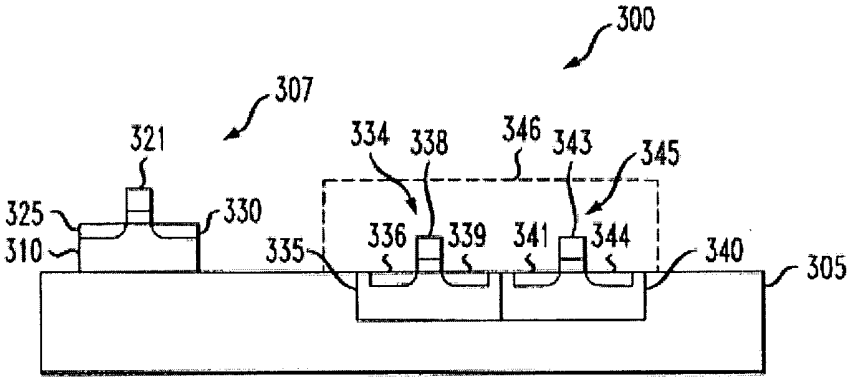

Illustration 1

FIG. 2F

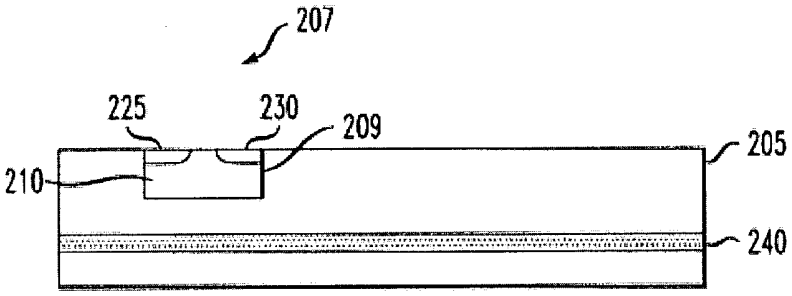

Illustration 2

VI. ISSUES

1) The first issue presented for consideration in this appeal is whether Claim 44, as rejected by the Examiner, fails to comply with the written description requirement under 35 U.S.C. §112, first paragraph.

2) The second issue presented for consideration in this appeal is whether Claims 44-47, 49-51 and 53, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over U.S. Patent No. 4,896,194 to Suzuki ("Suzuki") in view of U.S. Patent No. 5,672,889 to Brown ("Brown").

3) The third issue presented for consideration in this appeal is whether Claims 52 and 54, as rejected by the Examiner, are patentably nonobvious in accordance with 35 U.S.C. §103(a) over Suzuki in view of Brown, as applied to Claim 44 above, and further in view of U.S. Patent No. 5,326,991 to Takasu ("Takasu").

VII. GROUPING OF THE CLAIMS

Claims 44-47 and 49-54 do not stand or fall together. Claim 44 forms a first group, Claim 45 forms a second group, Claim 46 forms a third group, Claim 47 forms a fourth group, Claim 49 forms a fifth group, Claim 50 forms a sixth group, Claim 51 forms a seventh group, Claim 52 forms an eighth group, Claim 53 forms a ninth group, and Claim 54 forms a tenth group.

VIII. PRIOR ART

A. Suzuki

Suzuki, as shown in Illustration 3 below (FIG. 2b of Suzuki), is directed to a semiconductor device having an integrated circuit formed on a compound semiconductor layer. (Title) Suzuki teaches that a MOSFET may include a GaAs tub 31 located on a conductive substrate 32. Suzuki teaches that the conductive substrate 31 is a silicon substrate. Suzuki further teaches that a gate 36 may be formed on the GaAs tub 31, and that source and drain regions may be located within the GaAs tub 31. Suzuki further teaches that CMOS devices 39 and 40 may be formed on the conductive substrate 32.

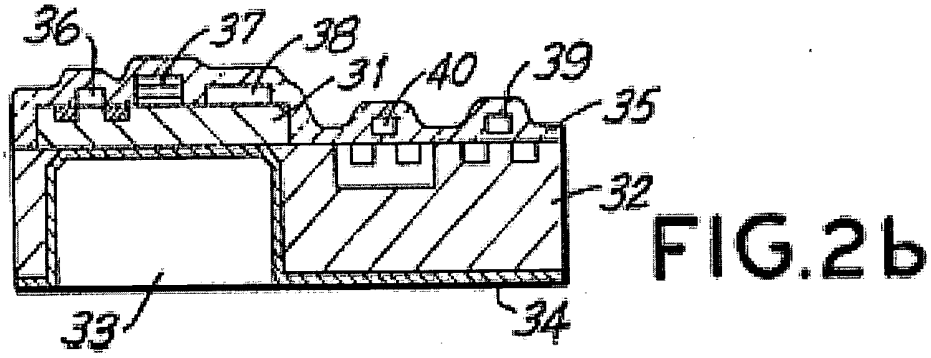

Illustration 3

B. Brown

Brown, on the other hand, is directed to a vertical channel silicon carbide metal-oxide-semiconductor field effect transistor with self-aligned gate for microwave and power applications. (Title) Brown further teaches a MOSFET formed in a silicon carbide tub, and the advantages of forming a power MOSFET in a silicon carbide material instead of a GaAs material.

C. Takasu

Takasu is directed to a semiconductor device having silicon carbide grown layers on insulating layers, and a MOS device. (Title). Takasu teaches that MOSFET devices may be formed over a SOI substrate.

IX. THE APPELLANTS' ARGUMENTS

The original specification contains support for the newly claimed elements of independent Claim 44. Further, the inventions set forth in independent Claims 44 and 54, and their respective dependent claims, are neither anticipated by nor made obvious from the references on which the Examiner relies.

A. Rejection of Claim 44 under 35 U.S.C. § 112, first paragraph

The Examiner currently rejects Claim 44 under 35 U.S.C. §112, first paragraph, asserting that it contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventors had possession of the claimed invention at the time

the application was filed. Specifically, the Examiner maintains that there is no support for a SiC tub located within a trench, as recited in Claim 44, since the embodiment of FIG. 3 (Illustration 1, above) does not disclose forming a trench. The Examiner's rejection is without support.

The Application does provide support for the SiC tub located within a trench, and located proximate CMOS devices. First, FIG.s 2A-D of the application (not shown), and their associated text, disclose a method for manufacturing a semiconductor device having a lateral metal-oxide semiconductor field effect transistor (MOSFET) 200, wherein the MOSFET 200 includes a SiC tub 210 located on a substrate 205. The specification, in the text associated with FIG. 2F (Illustration 2, above), then goes on to teach another embodiment where the SiC tub 210 is located within a trench 209. For example, the language describing FIG. 2F (Illustration 2, above) recites:

> FIGURE 2F illustrates still another embodiment, in which the MOSFET device 200 may be formed within a substrate 205 having an insulator layer 240 formed therein, which was discussed in FIGURE 2E. In such embodiments, a silicon trench 209 is conventionally formed in the substrate 205 prior to the formation of the silicon carbide layer 210. The silicon carbide layer 210 is then deposited in the silicon trench 209. Of course, another embodiment of the present invention may form the silicon trench 209 and the silicon carbide layer 210 within a substrate that does not have the insulator layer 240. Following the formation of the silicon carbide layer 210, a gate is formed on the silicon carbide layer 210 in the manner discussed herein for other embodiments. (Page 16, line 16 thru page17, line 4 of the application as filed).

If that were not enough, FIG. 3A (Illustration 1, above) and its related text goes on further to describe and show an embodiment where the device of FIG.s 2A-D is placed on a substrate proximate CMOS devices. While the specification does not specifically state that the configuration of FIG. 3A (Illustration 1, above) could also encompass the embodiment discussed with respect to

FIG. 2F (Illustration 2, above), the specification taken as a whole reasonably conveys to one skilled in the art that such a configuration is within the scope of the present invention. Therefore, the Appellants respectfully traverse the Examiner's rejection of the subject matter of Claim 44 under 35 U.S.C. §112, first paragraph, and in turn respectfully request respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 44.

B. Rejection of Claim 44 under 35 U.S.C. § 103

The combination of Suzuki and Brown fails to render obvious the elements of independent Claim 44, and its dependent claims, because the combination fails to teach or suggest every element of independent Claims 44. Specifically, the combination fails to teach or suggest a silicon carbide tub located within a trench formed in a conductive substrate, as recited in Claim 44, and as conceded by the Examiner. (Examiner's Action, page 5).

The Examiner agrees that neither Suzuki nor Brown specifically teaches or suggests this element, however, the Examiner continues to argue that it would have been obvious to a person of ordinary skill in the art to form the GaAs layer 31 in the Si substrate 32 rather than on the substrate 32, as disclosed in Suzuki. The Appellants disagree. The GaAs layer 31 of Suzuki cannot practically be formed in a trench in the substrate 32 because a substantial portion of the substrate 32 underlying the GaAs layer 31 is removed to form a hole 33 after the GaAs layer 31 is deposited on the substrate 32. (Column 3, lines 48-68). (Illustration 3, above). Forming the GaAs layer 31 in a trench in the substrate 32 and subsequently removing most of the portions of the substrate 32 under the trench would result in a device that was mechanically unsound and excessively susceptible to failure due to the lack of support of the GaAs layer 31 within the substrate 32. Thus, it is not

obvious to a person of ordinary skill in the art to form the GaAs layer 31 in a trench in the substrate 32.

Brown also fails to teach or suggest forming a silicon carbide tub within a trench formed in a conductive substrate, as recited in Claim 44 of the present application. In contrast, Brown merely teaches forming a number of different SiC layers 10, 12, 14 over one another, and then forming grooves 16 through at least two of the three SiC layers 10, 12, 14. (Column 5, lines 9-15). Thus, where the present invention requires the element of a silicon carbide tub located within a trench formed in a conductive substrate, Brown only discloses three SiC layers, one of which forms a silicon carbide tub. While Brown might teach trenches or grooves, the only material located within those trenches and groves in Brown are oxides and gate electrodes, but not the silicon carbide required by the present invention. Therefore, Brown also fails to teach or suggest that a silicon carbide tub is located within a trench in a conductive substrate, as presently claimed.

Moreover, because Brown is directed toward vertical transistors instead of horizontal transistors, one skilled in the art would find no suggestion, motivation or even mere mention of forming the SiC channel layer 12 in a trench in a substrate because a channel layer formed in a trench would cover or otherwise restrict access to the underlying source or drain and render the transistor inoperable.

The Examiner also asserts that the device of FIG. 2b (Illustration 3, above) of Suzuki is structurally identical to the device 307 of FIG. 3A (Illustration 1, above) of the present invention. The Examiner could not be any more incorrect. Among other differences, the device of FIG. 2b (Illustration 3, above) of Suzuki requires a huge cavity33 to be located under its silicon carbide layer

31. As indicated above, this huge cavity 33 prevents the silicon carbide layer 31 from being located in a substrate therebelow, as required by the present invention.

Accordingly, the combination of Suzuki and Brown fails to teach or suggest each and every element of Claim 44 of the present application. In view of the foregoing remarks, the combination of Suzuki and Brown fails to support a *prima face* case of obviousness of Claim 44 under 35 U.S.C. §103(a). Consequently, the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 44.

C. Rejection of Claim 45 under 35 U.S.C. §103

The Examiner has rejected Claim 45 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 45 additionally requires that the MOSFET has a breakdown voltage greater than an operating voltage of the CMOS device. The combination of Suzuki and Brown, however, does not teach or suggest that the MOSFET has a breakdown voltage greater than an operating voltage of the CMOS device, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 45. Accordingly, Claim 45 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 45.

D. Rejection of Claim 46 under 35 U.S.C. §103

The Examiner has rejected Claim 46 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 46 additionally requires that the MOSFET has a breakdown voltage of at least about 10 volts and the CMOS device has a breakdown voltage between about 3 volts and 5 volts. The combination of Suzuki and Brown, however, does not teach or suggest that the MOSFET has a breakdown voltage of at least about 10 volts and the CMOS device has a breakdown voltage between about 3 volts and 5 volts, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 46. Accordingly, Claim 46 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 46.

E. Rejection of Claim 47 under 35 U.S.C. §103

The Examiner has rejected Claim 47 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 47 additionally requires that the semiconductor device is a power converter and the MOSFET is a power switch for the power converter. The combination of Suzuki and Brown, however, does not teach or suggest that the semiconductor device is a power converter and the MOSFET is a power switch for the power converter, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 47. Accordingly, Claim 47 is nonobvious

over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 47.

F. Rejection of Claim 49 under 35 U.S.C. §103

The Examiner has rejected Claim 49 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 49 additionally requires that the silicon carbide tub is located over the conductive substrate. The combination of Suzuki and Brown, however, does not teach or suggest that the silicon carbide tub is located over the conductive substrate, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 49. Accordingly, Claim 49 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 49.

G. Rejection of Claim 50 under 35 U.S.C. §103

The Examiner has rejected Claim 50 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 50 additionally requires that the material is doped silicon, wherein the silicon is doped with a p-type dopant or an n-type dopant. The combination of Suzuki and Brown, however, does not teach or suggest that the material is doped silicon, wherein the silicon is doped with a p-type dopant or an n-type dopant, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie*

case of obviousness of dependent Claim 50. Accordingly, Claim 50 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 50.

H. Rejection of Claim 51 under 35 U.S.C. §103

The Examiner has rejected Claim 51 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 51 additionally requires that the source and drain regions are doped with a p-type dopant or an n-type dopant. The combination of Suzuki and Brown, however, does not teach or suggest that the source and drain regions are doped with a p-type dopant or an n-type dopant, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 51. Accordingly, Claim 51 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 51.

I. Rejection of Claim 53 under 35 U.S.C. §103

The Examiner has rejected Claim 53 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 53 additionally requires that the conductive substrate comprises silicon and the silicon carbide tub comprises a 3C silicon carbide. The combination of Suzuki and Brown, however, does not teach or suggest that the

conductive substrate comprises silicon and the silicon carbide tub comprises a 3C silicon carbide, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 53. Accordingly, Claim 53 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 53.

J. Rejection of Claim 52 under 35 U.S.C. §103

The Examiner has rejected Claim 52 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown, and further in view of Takasu. The above argument establishing the nonobviousness of independent Claim 44 is incorporated herein by reference. Dependent Claim 52 additionally requires that a buried oxide layer is formed in the conductive substrate. The combination of Suzuki, Brown and Takasu, however, does not teach or suggest that a buried oxide layer is formed in the conductive substrate, in combination with the base claim limitations. Thus, the combination does not establish a *prima facie* case of obviousness of dependent Claim 52. Accordingly, Claim 52 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 52.

K. Rejection of Claim 54 under 35 U.S.C. §103

The Examiner has rejected Claim 54 under 35 U.S.C. §103(a) as being unpatentable over the combination of Suzuki and Brown, and further in view of Takasu. The above argument establishing the nonobviousness of independent Claim 44 as well as the nonobviousness of dependent Claim 52

is incorporated herein by reference. Independent Claim 54 includes the element that a buried oxide layer is formed in the conductive substrate.

The Examiner asserts that it would have been obvious to a person of ordinary skill in the art to form a combination of the Suzuki and Brown devices on a SOI substrate as taught by Takasu in order to improve the electrical isolation of the device. The Appellants respectfully disagree.

As the Examiner concedes, neither Suzuki nor Brown teaches the insulator layer. Further, one skilled in the art would not be motivated to employ a SOI substrate as taught by Takasu with the teachings of Suzuki, as asserted by the Examiner. More specifically, after forming the GaAs layer 31 on the Si substrate 32, Suzuki teaches forming a hole 33 that terminates at the GaAs layer 31, wherein the sides of the hole 33 and the exposed, bottom surface of the GaAs layer 31 are subsequently lined with a metal layer 34 comprising a Ti/Au stack. (Column 5, lines 50-55). The metal layer 34 electrically connects the top and bottom sides of the device. One skilled in the art would not employ a SOI substrate or another substrate having a buried oxide layer therein when both sides of the substrate are electrically coupled to one another, because this would destroy the intended conductivity of the device. Thus, Suzuki fails to suggest employing a substrate having a buried oxide layer formed therein, as recited in Claim 54 of the present application.

Therefore, the combination of Takasu with Suzuki and Brown is improper, and thus does not teach or suggest these elements. Consequently, the combination does not establish a *prima facie* case of obviousness of independent Claim 54. Accordingly, Claim 54 is nonobvious over the combination and the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of Claim 54.

For the reasons set forth above, the Claims on appeal are patentably nonobvious over the references. Accordingly, the Appellants respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's Final Rejection of all of the Appellants' pending claims.

Respectfully submitted,

Hitt Gaines, P.C.

Greg H. Parker
Registration No. 44,995

Dated: 3-31-04

Hitt Gaines, P.C.
P.O. Box 832570
Richardson, Texas 75083-2570
(972) 480-8800
(972) 480-8865 (Fax)
E-Mail: greg.parker@hittgaines.com

X. APPENDIX A - CLAIMS

Claims 1-43 were previously canceled without prejudice or disclaimer.

44. A semiconductor device, comprising:

a lateral metal-oxide semiconductor field effect transistor (MOSFET), including:

a silicon carbide tub located within a trench formed in a conductive substrate;

a gate formed on the silicon carbide tub; and

source and drain regions located in the silicon carbide tub and laterally offset from the gate; and

a complimentary metal-oxide semiconductor (CMOS) device formed on the conductive substrate, the CMOS device having a tub comprising a material different from the silicon carbide tub.

45. The semiconductor device as recited in Claim 44 wherein the MOSFET has a breakdown voltage greater than an operating voltage of the CMOS device.

46. The semiconductor device as recited in Claim 44 wherein the MOSFET has a breakdown voltage of at least about 10 volts and the CMOS device has a breakdown voltage between about 3 volts and 5 volts.

47. The semiconductor device as recited in Claim 44 wherein the semiconductor device is a power converter and the MOSFET is a power switch for the power converter.

Claim 48 was previously canceled without prejudice or disclaimer.

49. The semiconductor device as recited in Claim 44 wherein the silicon carbide tub is located over the conductive substrate.

50. The semiconductor device as recited in Claim 44 wherein the material is doped silicon, wherein the silicon is doped with a p-type dopant or an n-type dopant.

51. The semiconductor device as recited in Claim 44 wherein the source and drain regions are doped with a p-type dopant or an n-type dopant.

52. The semiconductor device as recited in Claim 44 further comprising a buried oxide layer formed in the conductive substrate.

53. The semiconductor device as recited in Claim 44 wherein the conductive substrate comprises silicon and wherein the silicon carbide tub comprises a 3C silicon carbide.

54. A semiconductor device, comprising:

a lateral metal-oxide semiconductor field effect transistor (MOSFET), including:

a silicon carbide tub located within or contacting a conductive substrate;

a gate formed on the silicon carbide tub; and

source and drain regions located in the silicon carbide tub and laterally offset from the gate; and

a complimentary metal-oxide semiconductor (CMOS) device formed on the conductive substrate, the CMOS device having a tub comprising a material different from the silicon carbide tub, and wherein the conductive substrate includes a buried oxide layer formed therein.